

WHAT IS CLAIMED:

1 1. An integrated circuit switch comprising:
2 at least two signal ports coupled by a signal path, the signal path including a
3 channel of at least one series FET;
4 a shunt path coupled to ground and including a channel of a shunt FET; and
5 a control voltage applied to a gate of the series FET and to a drain/source of
6 the shunt FET.

1 2. A method for switching a signal so as to selectively connect a first port
2 in an integrated circuit to a second port in the integrated circuit, comprising:
3 providing a series switch in a signal path between the first port and the second
4 port;
5 providing a shunt switch in a shunt path coupled to ground; and
6 using a common logic signal to control both the series switch and the shunt
7 switch.

1 3. A switch for coupling a first port to a second port, comprising:
2 a control signal input;
3 at least one series FET connected in series between the first port and the
4 second port, said at least one series FET having a gate coupled to the control signal
5 input; and a shunt path including a shunt FET, the shunt FET having a drain and
6 source coupled to the control signal input and to the gate of said at least one series
7 FET, whereby a single control signal is applied to both said at least one series FET

8 and the shunt FET, via the control signal input, in order to turn said at least one series
9 FET on and simultaneously turn the shunt FET off and, conversely, in order to turn
10 the series FET off and simultaneously turn the shunt FET on.

1 4. The switch of claim 3, wherein the shunt FET includes a drain, source,
2 and a gate, the drain of the shunt FET is directly coupled to the gate of the series FET,
3 the source of the shunt FET is capacitively coupled to a ground reference, and the gate
4 of the shunt FET is coupled to the ground reference via a resistor for the control signal
5 reference.

1 5. The switch of claim 3, and further comprising at least one of a second
2 series FET or plurality of FETs in the signal path, with the gates of all series FETs
3 coupled to the control input.

1 6. A switch for coupling a first port to a second port, comprising:
2 a control signal input;
3 an FET connected in series between the first port and the second port, said
4 series FET having a gate coupled to the control signal input; and
5 means for enhancing the isolation between the first and second ports, and for
6 improving the harmonic noise rejection of the switch, the isolation and harmonic
7 rejection means having an input coupled to the control signal input and to the gate of
8 the series FET, whereby a single control signal is applied to both the series FET and
9 the isolation and harmonic rejection means, via the control signal input, in order to
10 turn the series FET on and simultaneously turn the isolation means off and,

11 conversely, in order to turn the series FET off and simultaneously turn the isolation
12 means on.

1 7. The switch of claim 6, wherein the isolation and harmonic rejection
2 means includes a shunt path including a shunt FET, the shunt FET having a drain
3 coupled to the control signal input and to the gate of the series FET, whereby the
4 single control signal is applied to both the series FET and the shunt FET, via the
5 control signal input, in order to turn the series FET on and simultaneously turn the
6 shunt FET off and, conversely, in order to turn the series FET off and simultaneously
7 turn the shunt FET on, the harmonic rejection is provided without the need of a
8 separate feedforward capacitor.

9 8. A method of controlling the coupling of a first port to a second port via
10 a series/shunt FET switch, comprising the steps of:

11 isolating the first port from the second port, using a single control signal, by
12 turning off a series FET by biasing the gate-source voltage of the series FET below
13 the pinchoff voltage, and by turning a shunt FET on by biasing the gate-source
14 voltage above the pinchoff voltage; and

15 coupling the first port to the second port, using a single control signal, by
16 turning on the series FET by biasing the gate-source voltage above the pinchoff
17 voltage, and turning the shunt FET off by biasing the gate-source voltage above the
18 pinchoff voltage.

1 9. An integrated circuit for selectively connecting and disconnecting a
2 first RF port to or from a second RF port, comprising:

3 a signal path connecting the first RF port and the second RF port;

4 at least one switching transistor having a signal path and a control electrode, a
5 first control voltage applied to the control electrode permitting a signal to pass, a
6 second control voltage applied to the control electrode rendering the current path to be
7 of high impedance; and

8 a shunt transistor having a diverging signal path, one end of the signal path of
9 the shunt transistor coupled to the control electrode (gate) of said at least one series
10 switching transistor, a second end of the signal path of the shunt transistor coupled
11 through a low signal impedance to the signal ground reference; additionally allowing
12 for control of the shunt transistor signal path impedance by application of the first
13 control voltage to both the control electrode (gate) of the series transistor and
14 simultaneously to the drain and/or source of the shunt transistor rendering the signal
15 path of the shunt transistor substantially nonconductive while the series transistor
16 signal path is conductive, and wherein application of the second control voltage to the
17 shunt transistor renders the signal path of the shunt transistor conductive while the
18 series transistor path is simultaneously nonconductive with the same second control
19 voltage simultaneously applied to its control electrode (gate) to thereby increase the
20 isolation between the first and second RF ports.

1 10. The integrated circuit of Claim 9, wherein said at least one switching
2 transistor is a field effect transistor.

1 11. The integrated circuit of Claim 9, wherein said at least one switching
2 transistor is an insulated gate field effect transistor.

1 12. The integrated circuit of Claim 10, wherein the signal path of said at
2 least one switching transistor extends from a first end coupled to the first RF port to a
3 second end coupled to the second RF port, the control electrode of said at least one
4 switching transistor comprising a gate, a feed-forward capacitor coupled from the first
5 end to the gate.

1 13. The integrated circuit of Claim 9, wherein the shunt transistor is a field
2 effect transistor.

1 14. The integrated circuit of Claim 13, wherein the shunt transistor is an
2 insulated gate field effect transistor.

1 15. The integrated circuit of Claim 14, wherein a drain of the shunt
2 transistor is coupled to the control electrode of said at least one switching transistor,
3 the first and second control voltages being applied to the drain.

1 16. The integrated circuit of Claim 14, wherein a source of the shunt
2 transistor is coupled to a gate of the series transistor by a resistor.

1 17. The integrated circuit of Claim 14, wherein a source of the shunt
2 transistor is coupled to an input for the first and second control voltages by a resistor.

1 18. The integrated circuit of Claim 9, wherein the signal path of the shunt
2 transistor is coupled to the signal ground reference through a shunt capacitor.

1 19. The integrated circuit of Claim 9, wherein an operational voltage input
2 is coupled to the signal path to provide a voltage differential across the series
3 transistors to the control input.

1 20. The integrated circuit of Claim 9, wherein the signal path includes the
2 current paths of a plurality of switching transistors, control electrodes of each of the
3 switching transistors commonly receiving the first or the second control voltages.

1 21. The integrated circuit of Claim 9, wherein the plurality of switching
2 transistors includes a first series field effect transistor having a signal path with one
3 end coupled to the first RF port, a second series field effect transistor having a signal
4 path with one end coupled to the second RF port, gates of the first and second series
5 field effect transistors coupled to an input for the first and second control voltages, a
6 feed-forward capacitor coupled between said signal path end and the gate of the first
7 series field effect transistor; and

8 said shunt transistor comprising a field effect transistor having a signal path
9 with a first end coupled to the gate of the second series field effect transistor, a second
10 end of the current path of the shunt transistor coupled to a ground reference through a
11 shunt capacitor, the shunt capacitor acting as a second feed-forward capacitor
12 associated with the second series field effect transistor.

13 22. The integrated circuit of claim 21 wherein between the first and second
14 series FETs may be a plurality of series FETs all using the same control voltage.

15 23. The integrated circuit of claim 9 wherein multiple series FETs are in series
16 between the first RF port and the said series switching transistor.